What is claimed is:

1. A semiconductor device comprising:

a first active region formed within a well;

a second active region formed within the well;

a channel region defined between the first active region and the second active region; and

a first active region interface having a center portion defining an interface from the first active region to the channel region and having a lower portion defining an interface from the first active region to a lower portion of the well, wherein the center portion of the active region interface provides a relatively smooth dopant transition from the first active region to the channel region.

2. The device of claim 1, wherein the first active region and the second active region are of n-type conductivity and the well is of p-type conductivity.

3. The device of claim 1, wherein the well further comprises a first pocket region located adjacent to the first active region and a second pocket region located adjacent to a second active region, wherein the first pocket region and the second pocket region have a greater magnitude of conductivity than the well.

4. The device of claim 1, wherein the first active region comprises a highly doped drain region, an extension region, and a source/drain region.

5. The device of claim 1, wherein the active region interface further comprises a surface portion that provides a relatively sharp dopant transition from the first active region to the channel.

6. The device of claim 1, further comprising a gate structure formed over the channel region between the first active region and a second active region.

7. The device of claim 6, further comprising first sidewall spacers comprised of oxide formed adjacent to the gate structure.

8. The device of claim 7, further comprising second sidewall spacers comprised at least partially of nitride and formed adjacent to the first sidewall spacers and being thicker than the first sidewall spacers.

9. The device of claim 6, further comprising a liner oxide covering at least a portion of a surface of the device.

10. A method of fabricating a semiconductor device comprising:

forming n-well regions within a PMOS region of the device and forming p-well regions within an NMOS region of the device;

forming gate structures in the PMOS and NMOS regions of the device;

masking the PMOS region;

implanting an n-type dopant into the NMOS region to form n-type highly doped drain regions;

performing a HALO implant of a p-type dopant into the NMOS region to form p-type pocket regions;

removing the mask from the PMOS region;

performing a blanket implant of an n-type dopant into the NMOS and PMOS regions forming a second HDD region within the NMOS region and a N+ region within the PMOS region;

masking the NMOS region;

implanting a p-type dopant into the PMOS region to form p-type highly doped drain regions;

performing a HALO implant of an n-type dopant into the PMOS region to form n-type pocket regions;

removing the mask from the NMOS region;

masking the PMOS region;

performing a n-type implant forming source/drain regions within the NMOS region;

removing the mask from the PMOS region and masking the NMOS region;

performing a p-type implant forming source/drain regions within the PMOS region; and

removing the mask from the NMOS region.

11. The method of claim 10, wherein the n-type highly doped drain regions are formed by implanting arsenic.

12. The method of claim 10, wherein the blanket implant employs phosphorous as the n-type dopant.

13. The method of claim 12, wherein the blanket implant is performed at about 4-8 keV energy and a dose of about $0.5x10^{13}$ - $2x10^{13}$.

14. The method of claim 10, further comprising forming first sidewall spacers adjacent to the gate structures prior to performing the blanket implant.

15. A method of fabricating a semiconductor device comprising:

forming a well region having a first conductivity within a semiconductor substrate;

forming gate structures over the well region;

implanting a first dopant at a first energy within selected portions of the well region forming highly doped drain regions;

forming HALO pocket regions by implanting a second dopant that has an opposite conductively of the first dopant;

implanting a third dopant at a second energy without a mask, wherein the third dopant is implanted with less energy than the first dopant and wherein the third dopant is more diffusible than the first dopant; and

diffusing the second dopant to create a relatively smooth dopant transition from the respective highly doped drain regions through the pocket regions to channel regions by performing additional processing, wherein the relatively smooth dopant transition reduces low power leakage.

16. The method of claim15, further comprising forming first sidewall spacers on the gate structures prior to implanting the first dopant.

17. The method of claim 16, further comprising forming second sidewall spacers on the gate structures prior to implanting the third dopant.

18. The method of claim 15, wherein the first implanted dopant is n-type.

19. The method of claim 15, wherein the first implanted dopant is n-type and the third implanted dopant is n-type.

20. The method of claim 15, wherein diffusing the second dopant by performing additional processing includes performing a deep source/drain implant of a fourth dopant.

21. The method of claim 15, wherein diffusing the second dopant further comprises forming a sharp dopant transition near surface and laterally from the highly doped drain region to a portion of the channel region that mitigates short channel effects.

22. A method of fabricating a semiconductor device comprising:

forming p-type wells within an NMOS region of a semiconductor substrate and forming n-type wells within a PMOS region of a semiconductor substrate;

forming gate structures on the p-type wells and the n-type wells;

implanting a first dopant at a first energy into the p-type wells, wherein the first dopant is n-type;

implanting a second dopant at an angle into the p-type wells forming p-type pocket regions, wherein the second dopant is p-type;

implanting a third dopant into both the NMOS region and the PMOS region at a second energy, wherein the second energy is less than the first energy and the third dopant is n-type;

implanting a p-type dopant into the n-type wells; and

implanting an n-type dopant at an angle into the n-type wells forming n-type pocket regions.

23. The method of claim 22, wherein the first dopant is arsenic, the second dopant is boron, and the third dopant is phosphorous.

24. The method of claim 22, further comprising implanting an n-type dopant into the p-type wells forming source/drain regions and at least partially diffusing the second dopant.

25. The method of claim 24, further comprising implanting a p-type dopant into the n-type wells forming source/drain regions.